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APPL NO.	FILING OR 371 (C) DATE	ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/779,904	02/17/2004	2133	770	02008.071003	38	3	3

22511
OSHA & MAY L.L.P.
1221 MCKINNEY STREET
HOUSTON, TX 77010

CONFIRMATION NO. 9608

FILING RECEIPT



OC000000012596650

Date Mailed: 05/11/2004

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

Masahiro Ishida, Tokyo, JAPAN;
Takahiro Yamaguchi, Tokyo, JAPAN;
Yoshihiro Hashimoto, Tokyo, JAPAN;

Domestic Priority data as claimed by applicant

This application is a DIV of 09/980,891 12/03/2001
which is a 371 of PCT/JP01/02910 04/04/2001

Foreign Applications

04
JAPAN 2000-101867 04/06/2000

If Required, Foreign Filing License Granted: 05/11/2004

Projected Publication Date: 08/19/2004

Non-Publication Request: No

Early Publication Request: No

Title

Method and apparatus for defect analysis of semiconductor integrated circuit

Docketing	
Action:	Reg. correct SFR
Base Date:	5-17-04
Due Date:	6-17-04
Deadline:	6-17-04
Initials:	JK
Atty/Sec. Initials:	

Preliminary Class

714

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Title 37, Code of Federal Regulations, 5.11 & 5.15**

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IFW

PATENT
ATTORNEY DOCKET NO. 02008/071003
U.S. PATENT APPLICATION NO. 10/799,904

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Masahiro ISHIDA, *et al.* Art Unit : 2133
Serial No. : 10/779,904 Examiner :
Filed : February 17, 2004
Title : METHOD AND APPARATUS FOR DEFECT ANALYSIS OF
SEMICONDUCTOR INTEGRATED CIRCUIT

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST TO CORRECT FILING RECEIPT

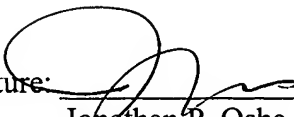
Applicants request that the filing date of the Japanese priority document be corrected from "04/06/2000" to --04/04/2000--.

Enclosed is a copy of the filing receipt as received from the PTO. The correct foreign priority information should be --Japanese Application No. 2000-101867, 04/04/2000--, as shown in the enclosed copy of the signed Declaration and Power of Attorney filed with this Divisional Patent Application on February 17, 2004.

Because this is a PTO error, no petition is believed necessary. However, if a petition is deemed to be required, please consider this paper as such and charge the appropriate fees to the Deposit Account 50-0591, reference No. 02008/071003.

If there are any other charges, or any credits, please apply them to the same Deposit
Account and reference No. 02008/071003.

Date: 5/27/04

Signature: 
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68271_1

CERTIFICATE OF MAILING BY FIRST CLASS MAIL (37 CFR 1.8)

Applicant(s): Masahiro ISHIDA, et al.

Docket No.

02008/071003

Serial No.

10/779,904

Filing Date

February 17, 2004

Examiner

Group Art Unit

2133

Invention: **METHOD AND APPARATUS FOR DEFECT ANALYSIS OF SEMICONDUCTOR INTEGRATED CIRCUIT**I hereby certify that this Request to Correct Filing Receipt

(Identify type of correspondence)

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(Date)Charlotte L. Cookingham

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